

IN THE DRAWINGS

Please amend FIGS. 4 and 5, as indicated on the attached marked-up copy of original FIGS. 4 and 5. No new matter is introduced.

REMARKS

The present application was filed on January 23, 2004 with claims 1 through 33. Claims 1 through 33 are presently pending in the above-identified patent application. Claims 1, 6, 17, 22, 27 and 32 are proposed to be amended.

In the Office Action, the Examiner objected to FIGS. 4 and 5 because symbols (Δ) and (X) were omitted in the legend boxes. Claim 8 was objected to as having the article "an" before "read only memory" instead of "a." Claims 6, 22 and 32 were rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. The Examiner rejected claims 1, 17 and 27 under 35 U.S.C. §102(b) as being anticipated by Fujitaka (United States Number 5,909,403). In addition, the Examiner indicated that claims 8-16 and 24-26 are allowed and that claims 2-5, 7, 18-21, 23, 28-31 and 33 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 6, 22 and 32 would be allowable if rewritten to overcome the section 112 rejections and to include all of the limitations of the base claim and any intervening claims.

Objection to Figures

The Examiner objected to FIGS. 4 and 5 because symbols (Δ) and (X) were omitted in the legend boxes. The drawings have been amended to include these labels. In addition, FIG. 5 has been amended to more clearly indicate the curve for "backgate only." Applicants respectfully submit that the addition of such labels to FIGS. 4 and 5 does not introduce new matter into the specification. Applicants respectfully request entry of the amendment to FIGS. 4 and 5, as indicated on the attached marked-up copy of original FIGS. 4 and 5 submitted herewith for the Examiner's approval, and request that the objection to the drawings be withdrawn.

Section 112 Objection and Rejection

Claim 8 was objected to as having the article "an" before "read only memory" instead of "a." Claim 8 has been amended in accordance with the Examiner's suggestion. Applicants respectfully request the withdrawal of this objection.

Claims 6, 22 and 32 were rejected under 35 U.S.C. §112 as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. In particular, the Examiner asserts that the recitation “wherein said biased gate voltage is applied only during a precharge phase” is inconsistent with pages 8 and 9.

The specification discusses two exemplary embodiments at pages 8 and 9. In a first embodiment, the raised source potential (i.e., the biased gate voltage) may be stable, not changing or varying between precharge and evaluation phases, nor between read and standby cycles. Thus, the same bias voltage is used for precharge and evaluation phases, as well as read and standby cycles. In a second exemplary embodiment, the source potential may be switched between the raised value and 0 volts. The raised value would be used during the precharge phase and during standby cycles. 0 volts would be used during the evaluation phase. Thus, the same raised bias voltage is used for precharge and standby phases and 0 volts is used for the evaluation phase.

Claims 6, 22 and 32 have been amended to emphasize that the biased gate voltage is applied only during a precharge phase of a read cycle, consistent with the second exemplary embodiment discussed above. It is noted that a read cycle comprises a precharge and an evaluation phase. Applicants respectfully request the withdrawal of this rejection.

Independent Claims 1, 17 and 27

Independent claims 1, 17 and 27 were rejected under 35 U.S.C. §102(b) as being anticipated by Fujitaka. With regard to claims 1, 17 and 27, the Examiner asserts that Fujitaka applies a biased gate voltage (to word line W1), relative to a source voltage (ground), to the gate of at least one transistor during a precharge phase (when PR signal is high in FIG. 4). It is noted that the 12 signals shown in FIG. 4 do not have the same time orientation. The second set of signals W1, S, N1, N2 correspond to when cell R11 is selected, and the third set of signals W0, S, N1, N2 correspond to when cell R3 is selected. In fact, only one word line Wn is active for each read operation. Thus, the signals W1 and W0 are not active at the same time and a biased gate voltage is only applied to one transistor in the array at a time.

The present invention, on the other hand, applies the biased gate voltage to each of a plurality of transistors in an array. See, e.g., FIG. 3 and corresponding discussion. Thus, Fujitaka does not disclose or suggest "applying a biased gate voltage, relative to a source voltage, to the gate of each of said plurality of transistors, said biased gate voltage to be applied at least during a precharge phase," as required by claim 1, as amended, or "a plurality of transistors each having a gate terminal adapted to be substantially simultaneously coupled to a biased gate voltage, relative to a source voltage, said biased gate voltage to be applied at least during a precharge phase," as required by claims 17 and 27, as amended.

Applicants respectfully request the withdrawal of the rejection of independent claims 1, 17 and 27.

Dependent Claims

The Examiner indicated that claims 8-16 and 24-26 are allowed.

In addition, claims 2-7, 18-23, and 28-33 were objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2-7, 18-23, and 28-33 are dependent on independent claims 1, 17 and 27, and are therefore patentably distinguished over Fujitaka because of their dependency from amended independent claims 1, 17 and 27 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims following entry of the amendments, i.e., claims 1-33, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,



Date: November 14, 2005

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FIG. 4

ROM CELL TRANSISTOR SUBTHRESHOLD LEAKAGE CURRENT
(N-CHANNEL, $V_d = 1.32\text{v}$)

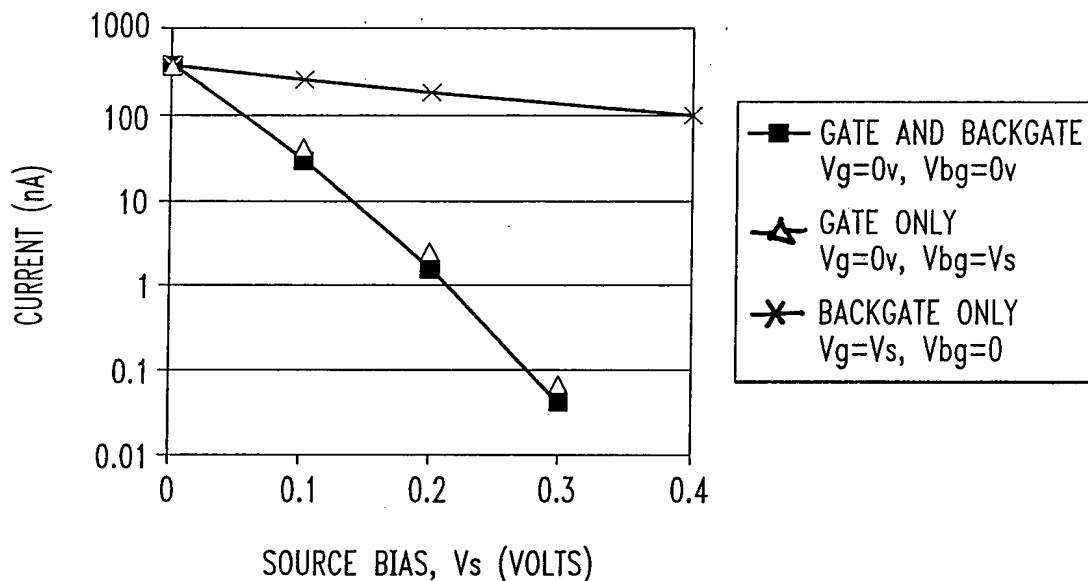


FIG. 5

ROM CELL TRANSISTOR SATURATION CURRENT
(N-CHANNEL, $V_d = 1.08\text{v}$)

